Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-46 (Canceled)

Claim 47 (New): A burn-in apparatus for burning-in semiconductor devices, comprising:

a semiconductor wafer comprising a plurality of unsingulated semiconductor devices on the wafer, each said semiconductor device comprising a plurality of resilient contact structures mounted thereon;

a test board comprising a plurality of contact elements, said test board disposed in proximity to said semiconductor wafer, forming pressure connections between ones of said resilient contact structures and corresponding contact elements of said test board; and

means for elevating a temperature of said semiconductor devices for a period of time.

Claim 48 (New): The burn-in apparatus of claim 47 wherein said test board comprises a printed circuit board.

Claim 49 (New); The burn-in apparatus of claim 47 wherein said contact elements of said test board further comprise a plurality of terminals mounted adjacent said test board.

Claim 50 (New): The burn-in apparatus of claim 47 further comprising means for positioning said wafer and said test board so that corresponding resilient contact structures and contact elements are aligned.

Claim 51 (New): The burn-in apparatus of claim 47 further comprising means for positioning said wafer and said test board so that corresponding resilient contact structures and contact elements are compressed together to form said pressure connections.

Claim 52 (New): The burn-in apparatus of claim 47, wherein said means for elevating is capable of elevating said temperature of said semiconductor devices to least 125° C.

Claim 52 (New): The burn-in apparatus of claim 47, wherein said means for elevating is capable of elevating said temperature of said semiconductor devices to least 125° C.

Claim 53 (New): The burn-in apparatus of claim 47, wherein said means for elevating is capable of elevating said temperature of said semiconductor devices to least 150° C.

Claim 54 (New): The burn-in apparatus of claim 47, wherein said means for elevating is capable of elevating said temperature of said semiconductor devices to least 175° C.

Claim 55 (New): The burn-in apparatus of claim 47, wherein said means for elevating is capable of elevating said temperature of said semiconductor devices to least 200° C.

Claim 56 (New): The burn-in apparatus of claim 47, wherein each of said plurality of resilient contact structures comprises:

(i) an attachment portion attached to a corresponding one of said semiconductor devices,

(ii) a resilient section, having an elongate springable shape, extending from said attachment portion, and

(iii) a contact region remote from said semiconductor device,

said resilient contact structure being free standing and said contact region being depressible towards said semiconductor wafer due to resilient spring action of said resilient section.

Claim 57 (New): The burn-in apparatus of claim 56, wherein said contact region comprises a contact tip structure joined to said resilient contact structure.

Claim 58 (New): The burn-in apparatus of claim 47 further comprising means for testing functionality of at least one of said semiconductor devices while at an elevated temperature.

Claim 59 (New): The burn-in apparatus of claim 47 further comprising means for testing a plurality of operating parameters of said semiconductor devices while at an elevated temperature.

Claim 60 (New): An apparatus comprising:

a semiconductor wafer comprising a plurality of unsingulated semiconductor devices on said wafer, said semiconductor devices comprising a plurality of resilient contact structures mounted thereon;

a test board comprising a plurality of contact elements, said test board disposed in proximity to said semiconductor wafer, forming pressure connections between ones of said resilient contact structures and corresponding contact elements of said test board; and

means for exercising at least one of said semiconductor devices.

Claim 61 (New): The apparatus of claim 60 further comprising means for elevating a temperature of said at least one semiconductor device while exercising said at least one semiconductor device.

Claim 62 (New): The apparatus of claim 61, wherein said means for elevating is capable of elevating said temperature of said at least one semiconductor devices to least 125° C.

Claim 63 (New): The apparatus of claim 60, wherein said means for exercising exercises said at least one semiconductor device by providing electrical signals through said contact elements of said test board to said ones of said resilient contact structures.

Claim 64 (New): The apparatus of claim 63 further comprising means for monitoring a response of said at least one semiconductor device to said electrical signals.

Claim 65 (New): The apparatus of claim 64 further comprising means for evaluating said response.